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Description

METHOD FOR IMPROVED ALIGNMENT OF MAGNETIC TUNNEL JUNCTION ELEMENTS

Background of Invention

[0001] The present invention relates generally to semiconductor device processing and, more particularly, to a method for improved alignment of magnetic tunnel junction elements.

[0002] Magnetic (or magneto-resistive) random access memory (MRAM) is a non-volatile random access memory technology that could potentially replace the dynamic random access memory (DRAM) and flash memory as the standard memory for computing devices. The use of MRAM as a non-volatile RAM will eventually allow for "instant on" systems that come to life as soon as the system is turned on, thus saving the amount of time needed for a conventional PC, for example, to transfer boot data from a hard disk drive to volatile DRAM during system power up.

[0003] A magnetic memory element (also referred to as a tunnel-

ing magneto-resistive, or TMR device) includes a structure having ferromagnetic layers separated by a non-magnetic layer (barrier), and arranged into a magnetic tunnel junction (MTJ). Digital information is stored and represented in the memory element as directions of magnetization vectors in the magnetic layers. More specifically, the magnetic moment of one magnetic layer (also referred to as a reference layer) is fixed or pinned, while the magnetic moment of the other magnetic layer (also referred to as a "free" layer) may be switched between the same direction and the opposite direction with respect to the fixed magnetization direction of the reference layer. The orientations of the magnetic moment of the free layer are also known as "parallel" and "antiparallel" states, wherein a parallel state refers to the same magnetic alignment of the free and reference layers, while an antiparallel state refers to opposing magnetic alignments therebetween.

[0004] Depending upon the magnetic state of the free layer (parallel or antiparallel), the magnetic memory element exhibits two different resistance values in response to a voltage applied across the tunnel junction barrier. The particular resistance of the TMR device thus reflects the magnetization state of the free layer, wherein resistance is

"low" when the magnetization is parallel, and "high" when the magnetization is antiparallel. Accordingly, a detection of changes in resistance allows a MRAM device to provide information stored in the magnetic memory element (i.e., a read operation). In addition, a MRAM cell is written to through the application of a bi-directional current in a particular direction, in order to magnetically align the free layer in a parallel or antiparallel state.

[0005] MRAM devices, like semiconductor devices in general, are continually becoming smaller in size and require manufacturing processes that are capable of producing these devices. Alignment techniques are implemented during manufacturing processes in order to ensure correct alignment of the various layers within semiconductor devices. Typically, alignment marks are utilized in the layers to help align the various features.

[0006] In the context of MRAM devices, the MTJ stacks require extremely smooth substrates for deposition thereon, in order to create a near-planar tunnel barrier such that the very small coherence lengths of the spin-polarized electrons will be uniform across the device. Since this MTJ stack is non-transparent to light, the lithography on top of this layer requires topographic (rather than material

contrast) features for alignment and overlay measurement through the layer. Because the underlying layer is typically chemically mechanically polished (CMP) as a final step before MTJ stack deposition, conventional alignment mark formation in this regard also typically leaves slurry residue trappings from smoothing CMP operations within the alignment mark topography. This (along with dished marks) makes alignment difficult. In addition, across-the-wafer inhomogeneity inherent to most CMP processes leaves uncontrollable amounts of tantalum nitride (TaN) film. This results in device shorting for cross-point array architectures.

SUMMARY OF INVENTION

[0007] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for aligning an opaque, active device in a semiconductor structure. In an exemplary embodiment, the method includes forming an opaque layer over an optically transparent layer formed on a lower metallization level, the lower metallization level including one or more alignment marks formed therein. A portion of the opaque layer is patterned and opened corresponding to the location of the one or more alignment marks in the lower metalliza-

tion level so as to render the one or more alignment marks optically visible. The opaque layer is then patterned with respect to the lower metallization level, using the optically visible one or more alignment marks.

[0008] In still another aspect, a method for aligning a magnetic tunnel junction (MTJ) element in a semiconductor memory array includes forming an MTJ stack layer over an optically transparent layer formed on a lower metallization level, the lower metallization level including one or more alignment marks formed therein. A portion of the MTJ stack layer is patterned and opened corresponding to the location of the one or more alignment marks in the lower metallization level so as to render the one or more alignment marks optically visible. The MTJ stack layer is then patterned with respect to the lower metallization level, using the optically visible one or more alignment marks.

Brief Description of Drawings

[0009] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

[0010] Figure 1 is a view of a series of conventionally formed alignment marks characterized by dishing;

[0011] Figure 2 is a cross-sectional view of a processing stage of an MRAM device, during which a magnetic stack material

is deposited for MTJ formation and subsequent alignment to a given metallization level, in accordance with an embodiment of the invention;

[0012] Figure 3 illustrates the MRAM device following etching of the oxide layer, TiN hardmask and MTJ stack layer according to the pattern shown by the lithography step of Figure 2;

[0013] Figure 4 is an SEM cross-section of an exemplary alignment mark that becomes optically visible through a covering TaN layer, following the hardmask/MTJ stack etch sequence shown in Figure 3;

[0014] Figure 5 illustrates a protective oxide hardmask layer that may first be formed over the device prior to the MTJ stack patterning;

[0015] Figure 6 illustrates MTJ lithography using a modified kerf, wherein the areas previously opened during the etch step(s) of Figure 3 are also covered with hardened resist;

[0016] Figures 7(a) and 7(b) illustrate exemplary 2D and 1D alignment marks, respectively, opened up using the presently disclosed process; and

[0017] Figure 8 is an SEM illustrating a plurality of magnetic tunnel junctions aligned and patterned in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0018] The alignment of active devices to an associated bitline/wordline underneath the device is a prerequisite for making dense arrays for superior performance of the semiconductor device. For example, in 0.18 micron logic technology, the required alignment is on the order of less than 70 nanometers (nm) for any two layers of the device, in order for the design to work.

[0019] MRAM device formation (in particular, magnetic tunnel junction etching) is one example of a non-interconnect, back end of line (BEOL) metal etch. Here, topography from prior levels is undesirable for device functionality. A very rough tunnel junction interface is capable of lowering the signal available for discriminating between the two logic states. However, a very minimal residual topography that is insufficient for precise alignment (10's of nanometers), is available from the CMP processes that create the underlying levels. These levels of wiring are used to carry the currents required to switch the devices. Very precise alignment of the MTJs to these levels is required for tight control of the switching characteristics of the device.

[0020] In the formation of MRAM devices, the alignment of the magnetic tunnel junction (MTJ) stacks to the metal line

underneath poses a particularly tricky problem since the MTJ stack itself is opaque. Proper alignment, which is achieved through the use of a lithographic stepper prior to printing of the pattern, is based on the accurate detection of reflected light from the alignment structures etched on the layer underneath. The position of the alignment marks is calculated and the wafer is thus positioned accurately on the stage by the stepper feedback mechanism.

[0021] However, because the MTJ stack materials are opaque, reflected light does not contain information about the underlying alignment structures. Accordingly, one way this problem has been addressed in the past is through the creation of surface topography with the alignment marks, as discussed above, in order to align opaque junctions. The formation of such alignment marks with topographic characteristics can be implemented by etching out copper alignment marks using a tantalum nitride (TaN) hardmask, followed by removal of the TaN by chemical mechanical polishing (CMP), and deposition of the magnetic stack and hardmask layers. The resultant topography on the MTJ stack is employed for alignment. Again, this approach may result in slurry trapping in the alignment marks dur-

ing prior TaN CMP, thus making alignment rather difficult. In some cases, the alignment marks can become badly dished by non-uniform CMP, thus making it very difficult or impossible to use for alignment purposes, as is illustrated in Figure 1.

[0022] Therefore, in accordance with an embodiment of the invention, there is disclosed a method of alignment of opaque active devices in dense semiconductor arrays wherein alignment marks are utilized optically without any topography, thereby eliminating the above described disadvantages. Briefly stated, a block out mask is formed after the opaque stack is deposited in order to open up alignment marks present thereunderneath, in a manner that they become optically visible to the aligning apparatus.

[0023] Referring now to Figure 2, there is shown a cross-sectional view of a processing stage of an MRAM device 100, during which the magnetic stack material is deposited for MTJ formation and alignment to a given metallization level. It should be understood that although the alignment methodology presented herein is in the context of MRAM device processing, it is equally applicable to other types of semiconductor structures in which alignment of opaque

active elements is carried out. As is particularly shown in Figure 2, an optically transparent layer 102 of TaN is deposited on top of a metallization level 104 (e.g., M2 or M1 depending on the specific device structure). Shown in the metallization level 104 is an exemplary metal line 106 (e.g., copper) to which the subsequently formed MTJ devices will be aligned, as well as a plurality of metal filled alignment marks 108. The deposition of the TaN layer 102 is followed by the individual layers comprising the opaque MTJ stack layer (denoted collectively at 110), and a hard-mask 112 (e.g., titanium nitride (TiN)) to enable etching of the MTJ devices.

[0024] Next, a block out mask is used for a lithography step, in which an alignment pattern is opened in a photoresist layer 114, over the top of the alignment marks 108 of metallization level 104. The active device regions of the wafer are protected by photoresist at this stage. This block out mask step need not be aligned using EGA (Enhanced Global Alignment), since the desired tolerance for this purpose is only on the order of microns, as opposed to about 70 nm as in the case of other alignment steps. Accordingly, any generated topography during the formation of metallization level 104 should be sufficient

to carry out a coarse alignment of the block out mask. In the case of FET based MRAM device architectures, this alignment may be carried out using prior via level topography.

[0025] As shown in Figure 3, the pattern printed by the lithography step of Figure 2 is etched through TiN hardmask 112 and MTJ stack layer 110, thereby opening a window 116 atop the portion of the TaN layer 102 over the alignment marks 108. The TiN hardmask 112 may be opened in a metal etch chamber using a suitable chemistry. Furthermore, the MTJ stack layer 110 may be etched using a suitable chemistry to stop on the TaN layer 102. Thus, at this point during the processing, the alignment marks 108 on metallization level 104 are optically visible through the TaN layer 102. Figure 4 is an SEM cross-section of an exemplary alignment mark that is optically visible through a covering TaN layer, following the hardmask/MTJ stack etch sequence.

[0026] Since the alignment marks 108 are now visible following the above described etching, the MTJ stack may now be patterned in alignment to better than 70 nm over the metal line 106. During the MTJ device formation, both the patterned MTJ devices and the etched alignment area over

the alignment marks 108 will be protected from the MTJ etch by hardened resist. Optionally, a protective oxide hardmask layer 118 may first be formed over the device prior to the MTJ stack patterning, as shown in Figure 5. The MTJ device lithography is then carried out using a modified kerf, wherein the areas previously opened during the etch step(s) of Figure 3 are also covered with hardened resist 120 in addition to the MTJ stack area, as shown in Figure 6. This also serves to protect that portion of the oxide hardmask layer 118 over the alignment marks 108 during the subsequent oxide open portion of the MTJ stack formation.

[0027] In order to implement the resist patterning of Figure 6, a modified MTJ patterning mask is used that serves the dual purpose of patterning the MTJ devices and protecting the exposed kerf area containing the alignment marks 108. Accordingly, during the MTJ patterning (including oxide hardmask opening, TiN hardmask opening and stack patterning), the optional oxide hardmask layer 118 above the alignment marks 108 is protected by resist 120, while during the TiN open process (which employs a Cl chemistry), the copper alignment marks 108 are protected by the oxide/TaN process. Finally, during the MTJ stack etch

itself, the TaN layer 102 (and some oxide material, if used) continue to protect the copper alignment marks 108.

[0028] As will be appreciated, the alignment of the MTJ devices to the copper alignment marks 108 is now much easier since they are optically visible through the resist and TaN layer 102. Figures 7(a) and 7(b) illustrate exemplary 2D and 1D alignment marks, respectively, opened up using the above process. As compared with the dished out topography alignment marks of Figure 1, the optically visible marks shown in Figures 7(a) and 7(b) provide superior stability and alignment capability of opaque materials without resorting to topographic assistance, which is inherently unstable and requires additional etching and CMP steps. Finally, Figure 8 is an SEM illustrating a plurality of (elliptically shaped) magnetic tunnel junction devices 122 aligned and patterned using the above described process. The wordlines (denoted as M1) may be clearly seen beneath the junctions 122, wherein the alignment thereof is in the order of less than 70nm between the junctions and the M1 lines.

[0029] Through the use of the above described optical alignment process, any active device may be aligned to layers there-

underneath as demanded by design criteria for dense arrays. While particularly suited for MRAM device processing, the method may be extended to any device that is opaque in nature and needs alignment to a prior level, and without the need for special planarization to induce critical topography. In the case of MRAM, this method provides excellent alignment of opaque magnetic tunnel junctions to metal levels underneath, thus allowing for shrinkage of the circuitry. Moreover, this process eliminates the requirement for a thick TaN hardmask during wet etching of topographic alignment marks, as well as an associated CMP to finally reduce the TaN thickness.

[0030] Still a further advantage stems from the fact that pad-to-pad shorting of the metal lines underneath the active devices are eliminated, since a TaN hardmask is not required in this scheme. Heretofore, this has been a major yield detractor for cross-point architecture MRAM devices. In addition, for FET-based architectures, the process allows for damascene formation of the local strap level to be in alignment with the metal underneath. This method is also stacking friendly, in the sense that several layers of alternate MTJ and metal wiring lines may be built using this process.

[0031] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.